

1 Description

2

3 Device and method for measuring individual cell voltages in
4 a cell stack of an energy accumulator.

5

6 The invention relates to a device for measuring individual
7 cell voltages in a cell stack of an energy accumulator,
8 especially of an energy accumulator in a motor vehicle
9 electrical system.

10

11 The invention also relates to a method for operating this
12 device.

13

14 In motor vehicle electrical networks, as well as today's
15 usual lead acid accumulators, other energy accumulators also
16 constructed from individual cells will be used, for example
17 nickel-metal-hydride accumulators, Lithium-Ion accumulators
18 and double-layer capacitors.

19

20 In lead-acid accumulators the charge provided of the
21 individual cells of the accumulator is balanced out by a
22 slight overcharging of the accumulator as a whole until such
23 time as all cells are finally charged.

24

25 Balancing the charge between a weakly-charged accumulator

1 and the group of the remaining accumulators in a plurality
2 of series-connected accumulators by means of a square-wave
3 generator which is connected to these accumulators via a
4 transformer is known from EP 0 432 639 A2.

5

6 With the new types of energy accumulator mentioned however
7 the sensitivity of the individual cells to overcharging or
8 overvoltage is a problem. In contrast to lead-acid
9 accumulators, with a lithium-ion accumulator for example the
10 charge voltage of a cell cannot significantly exceed a value
11 of around 4.2V since otherwise the danger of destruction or
12 even of the cell catching fire arises. With double-layer
13 capacitors the maximum charge voltage is about 2.5 to 2.7V.

14

15 As a result of production-related differing variation of the
16 self-discharge of the cells, the charge states and cell
17 voltages in a cell stack will assume different values over
18 longer periods of operation.

19

20 One problem here is that as a rule only the overall voltage
21 of the cell stack, i.e. of the energy accumulator, can be
22 recorded as the pole voltage, but not the voltage of each
23 individual cell. Thus charge balancing can only be
24 undertaken periodically "on suspicion". If however an
25 increased self-discharge - such as towards the end of the

1 life of the energy accumulator - or an error in a individual
2 cell occurs, for example a short circuit, this cannot be
3 detected immediately. The result of this can be that during
4 the next charge process the charge voltage is divided
5 between fewer cells, so that individual cells are subjected
6 to an increased voltage. This then leads to the destruction
7 of further cells and must be avoided in any event.

8

9 It is therefore very desirable to know the voltages of the
10 individual cells in a cell stack of such an energy
11 accumulator in order to be able to react in the appropriate
12 manner.

13

14 The measurement of the individual cell voltages is difficult
15 since only the lowest cell has a ground reference point,
16 meaning that it can be recorded with reference to ground
17 (reference potential) whereas for all other cells a
18 conversion to ground potential is necessary in order to be
19 able for example to detect them via the analog/digital
20 converter of a microcontroller.

21

22 The object of the invention is to create a device to measure
23 the voltages of the individual cells of a cell stack in an
24 energy accumulator. Another object of the invention is to
25 specify a method for operating this device.

1 According to the invention this object is achieved by a
2 device in accordance with the features of claim 1 and a
3 method in accordance with the features of claim 3.

4

5 Embodiments according to the invention are explained below
6 in more detail with reference to a schematic drawing.

7

8 Advantageous developments of the invention can be taken from
9 the subclaims.

10

11 The drawing shows the following:

12

13 Figure 1 a basic circuit diagram of a device for
14 measurement of the cell voltages of a cell stack consisting
15 of a number of cells,

16

17 Figure 2 a detailed circuit diagram of a first device for
18 measurement of the voltage of an individual cell,

19

20 Figure 3 input and output signals of the differential
21 amplifier Diff1 used in the first circuit,

22

23 Figure 4 input and output signals of the synchronous
24 rectifier Amp1 used in the first circuit,

25

1 Figure 5 a detailed circuit diagram of a second device with
2 an alternative synchronous rectifier Diff2,

3

4 Figure 6 input and output signals of the differential
5 amplifier Diff1 used in the second circuit,

6

7 Figure 7 input and output signals of the synchronous
8 rectifier Diff2 used in the second circuit 2.

9

10 Figure 1 shows a basic circuit diagram of an inventive
11 device to measure individual cell voltages in a cell stack
12 of an energy accumulator. The Figure shows a cell stack ZS
13 with series-connected cells Z1, Z2 to Zn of a lithium-ion
14 accumulator for example, with the cell connections (plus and
15 minus pole) being brought out. Further details are discussed
16 more closely below.

17

18 The invention will be explained initially with reference to
19 a device for voltage measurement at an individual cell in
20 accordance with a detailed circuit diagram shown in Figure
21 2.

22

23 Figure 2 shows a device to measure the voltage of an
24 individual cell Z1 of the cell stack ZS shown in Figure 1,
25 for example of a lithium-ion accumulator with a cell voltage

1 Uz=4.2V, of which the minus pole is connected to reference
2 potential GND.

3

4 Arranged in parallel to this cell Z1 is a series circuit of
5 two diodes D1a and D1b which conduct current in the
6 direction from the minus pole to the plus pole of the cell
7 Z1.

8

9 The connection point of the two diodes D1a and D1b is linked
10 via a capacitor C1 to the non-inverting input of a
11 differential amplifier Diff1.

12

13 A reference circuit REF features two series-connected diodes
14 D3 and D4, with the anode of the one diode - D4 - being
15 connected to reference potential GND and to the cathode of
16 the other diode - D3.

17

18 The connection point of the two diodes D3 and D4 is
19 connected via a capacitor C3 to the inverting input b of the
20 differential amplifier Diff1, of which the output c leads to
21 the input of a rectifier, which in this exemplary embodiment
22 is embodied as a synchronous demodulator (Amp1, R1 to R3 and
23 S1) of which more details will be provided below.

24

25 The method in accordance with the invention for operating

1 this device works as follows:

2

3 Two alternating current sources I1 and I2 are controlled by
4 an oscillator clock T1 of an oscillator not shown in Figure
5 2, of which the first alternating current source I1,
6 arranged between the non-inverting input of the differential
7 amplifier Diff1 or the capacitor C1 and reference potential
8 GND, injects an alternating current into the capacitor C1,
9 while the second alternating current source I2, arranged
10 between the inverting input of the differential amplifier
11 Diff1 or the capacitor C3 and reference potential GND
12 injects an alternating current into the capacitor C3 of the
13 reference circuit REF.

14

15 Alternating current source I1 applies a square-wave
16 alternating current of for example $\pm 100\mu\text{A}$ to the capacitor
17 C1 The clock frequency in this case is to be selected so
18 that it is high enough for the capacitor not to be
19 significantly charged or discharged during the period of
20 oscillation.

21

22 The input and output signals of the differential amplifier
23 Diff1 and of the operational amplifier Amp1 are shown in
24 Figures 3 and 4 to which reference will be made during the
25 course of the description.

1 The signals in Figures 3, 4, 6 and 7 are shown in the steady
2 state in each case.

3

4 With a positive current the voltage at the two terminals of
5 the capacitor C1 will increase until such time as the diode
6 D1a becomes conductive; with negative current the voltage at
7 the two terminals of the capacitor will decrease until such
8 time as the diode D1b becomes conductive.

9

10 This thus produces a square-wave alternating voltage for
11 which the peak-to-peak value in the steady state corresponds
12 to the cell voltage U_z , multiplied by the on-state voltages
13 U_d of the two diodes D1a and D1b: $V_1 = U_z + 2U_d = 4.2V +$
14 $2*0.64V = 5.48V = \pm 2.74V$ (see Figure 3a).

15

16 The alternating current source I_2 drives the capacitor C_3
17 with the same capacitance ($C_3 = C_1$) and current value $\pm 100\mu A$
18 via the on-state voltages of the two diodes D3 and D4. Since
19 these two diodes are connected to reference potential GND,
20 the alternating voltage here amounts to $V_2 = 0V + 2*0.64V =$
21 $1.28V = \pm 0.64V$ (see Figure 3b). This is the alternating
22 voltage reference.

23

24 The difference $V_1 - V_2$ is now formed in the differential
25 amplifier Diff1: $V_1 - V_2 = 5.48V - 1.28V = 4.2V$. Since the

1 differential amplifier in this exemplary embodiment for
2 example has an amplification factor of "2", an alternating
3 voltage of $8.4V = \pm 4.2V$ appears at its output c (see Figure
4 3c).

5

6 The output voltage of the differential amplifier Diff1 is
7 now fed to the synchronous demodulator Amp1. The modulator's
8 input signal at the inverting input corresponds to the
9 output signal of the differential amplifier Diff1 (Figure 4a
10 = Figure 3c).

11

12 The synchronous demodulator consists of an operational
13 amplifier Amp1, resistors R1 to R4 and a capacitor C4. A
14 switch S1 is arranged between the non-inverting input of the
15 operational amplifier Amp1 and reference potential GND,
16 which is switched over by the oscillator clock T1 (Figure
17 4b).

18

19 When switch S1 is open (positive amplitude of the square-
20 wave signal) the operational amplifier Amp1 has an
21 amplification factor of "+1", when switch S1 is closed
22 (negative amplitude of the square-wave signal), it has a
23 factor of "-1". Figure 4b indicates how switch S1
24 periodically connects the non-inverting input of the
25 operational amplifier Amp1 to reference potential and thus

1 switches over the amplification factor.

2

3 The output signal V_0 at the output of the circuit follows
4 the output signal of the operational amplifier $Ampl_1$,
5 filtered by a filter formed from the resistor $R4$ and
6 capacitor $C4$, in which case any switching problems are
7 eliminated. The output signal V_0 corresponds to the voltage
8 U_z of the cell $Z1$ and can be tapped at the output of the
9 synchronous demodulator, related to reference potential GND
10 (or ground potential, $0V$).

11

12 Figure 5 shows a further detailed switching diagram as shown
13 in Figure 2 but with an alternate version of the synchronous
14 demodulator consisting of the components $Diff2$, $S2$, $S3$, $C5$
15 and $C6$.

16

17 The circuit from the cell $Z1$ via the diodes $D1a$, $D1b$, $D3$,
18 $D4$, the capacitors $C1$ and $C3$ as well as the alternating
19 current sources $I1$ and $I2$ up to the output of c of the
20 differential amplifier $Diff1$ corresponds to the circuit
21 shown in Figure 2. The input signals at the inputs a (Figure
22 6a) and b (Figure 6b) correspond to those shown in Figure 3a
23 and 3b.

24

25 The output signal at output c of the differential amplifier

1 Diff1 is connected by means of two parallel switches S2 and
2 S3 with the oscillator clock T1
3 - alternately to a capacitor C5 as well as the non-
4 inverting input of a further differential amplifier
5 Diff2, or
6 - to a capacitor C6 as well as to the inverting input b of
7 the further differential amplifier Diff2

8

9 For a positive amplitude of the oscillator clock T1 switch
10 S2 is closed (conductive) and switch 3 opened; For a
11 negative amplitude of the oscillator clock T1 switch S3 is
12 closed and switch 2 is opened. This means that capacitor C5
13 is charged at the positive value (Figure 7b) and capacitor
14 C6 at the negative value (Figure 7b) of the alternating
15 voltage output signal appearing at the output c of the
16 differential amplifier Diff1 (Figure 7a = Figure 6c).

17

18 The further differential amplifier Diff2 now forms the
19 difference between the two direct currents present at its
20 inputs a and b (in the Example: +2.10V and -2.10V = 4.20V:
21 Figure 7c), which can be tapped at its output c as grounded
22 direct current V=, which corresponds to the cell voltage Uz.

23

24 Whereas Figures 2 and 5 each show a detailed circuit diagram
25 for measuring an individual cell voltage to enable the

1 method to be better explained, Figure 1 shows a basic
2 circuit diagram of an inventive device to measure a
3 plurality of cell voltages in a cell stack of an energy
4 accumulator.

5

6 The Figure shows a cell stack ZS with series-connected cells
7 Z1, Z2 to Zn of a lithium-ion accumulator for example.
8 Arranged in parallel to each cell is the series circuit of
9 two diodes D1a-D1b to Dna-Dnb which conduct current in the
10 direction from the minus pole to the plus pole of the cell.

11

12 The connection points of the two diodes D1a-D1b to Dna-Dnb
13 assigned to a cell in each case are routed via a capacitor
14 C1 to Cn to the terminals of a changeover switch UM which
15 connects them in turn, controlled by a divider signal T2 of
16 a clock control ST, to its output.

17

18 The clock control ST consists of an oscillator OSZ which
19 creates an oscillator clock signal T1, a square wave
20 alternating voltage of a specific frequency, which is
21 stepped down by means of a frequency divider DIV into a
22 divider signal T2 in order to continue to switch the
23 changeover switch UM after the cell voltage has been
24 successfully detected.

25

1 The changeover switch UM must feature a number of switch
2 positions corresponding to the number of cells of the cell
3 stack, which (with the double layer capacitors) can reach an
4 order of magnitude of between 20 and 30. This changeover
5 switch can for example be embodied as a CMOS switch.

6

7 The two alternating current sources I1 and I2 known from
8 Figure 2 are controlled by the oscillator clock T1 of the
9 oscillator OSZ of which the first alternating current source
10 I1 injects an alternating current via the changeover switch
11 UM depending on its switch setting in to one of the
12 capacitors C1 or C2 to Cn, while the second alternating
13 current source I2 injects an alternating current into the
14 capacitor C3 of the reference circuit REF, which as well as
15 this capacitor C3, again features two diodes D3 and D4 of
16 which the connection point is connected to the capacitor C3.

17

18 The output of the changeover switch UM and of the terminal
19 of the capacitor C3 not connected to the diodes D3, D4 are
20 connected to the inputs a and b of the differential
21 amplifier Diff1, of which the output c is connected to a
22 rectifier GLR controlled by the oscillator clock T1, at the
23 output of which a direct current V= proportional to the
24 relevant cell voltage Uz appears consecutively.

25

1 The rectifier GLR can be embodied as a synchronous
2 demodulator Amp1 or Diff2 shown in Figure 2 or Figure 5.

3

4 The output signal V_+ of the rectifier GLR corresponds in the
5 steady state to the voltage U_z of the cell selected in each
6 case with the changeover switch U_M , but now shifted in
7 potential with reference to ground GND.

8

9 Accordingly with each advance of the changeover switch U_M ,
10 the corresponding cell voltage is presented at the output of
11 the rectifier GLR. As a result the individual cell voltages
12 are mapped consecutively in relation to ground.

13

14 To monitor the cell voltages the voltage sequence can be
15 compared in the simplest case to a lower and an upper value
16 with a limit value comparator. Exceeding the maximum value
17 indicates an overvoltage of the cell here; Dropping below a
18 minimum value indicates a short circuit. This information
19 can now be fed to a monitoring unit which takes appropriate
20 measures in response to it; such as aborting the charging
21 process, initiating a new charge balancing process or
22 sending information to the driver telling them that a visit
23 to the workshop is required.

24

25 Supervision using limit value comparators is however very

1 approximate. The cell involved cannot be identified for
2 example. Also with a charge balancing process the point at
3 which charging equilibrium has been achieved cannot be
4 detected.

5

6 In a refined supervision using a microcontroller the voltage
7 values $V=$ can be recorded chronologically one after the
8 other with reference to the switching clock of the
9 changeover switch so that a further evaluation of the cell
10 voltage can be undertaken using supervision software.

11

12 In charge balancing the slow balancing of the individual
13 cell voltages is detectable so that the ending of the charge
14 or discharge process can be defined.

15

16 A long-term supervision of the individual cells is also
17 possible so that - on detection of the fall in the capacity
18 of a cell, an increase of the self-discharge or an increase
19 of the internal resistance of a cell - a warning message can
20 be issued indicating that a trip to the workshop is
21 necessary.

22

23 This increases the reliability of the system quite
24 significantly and reduces the repair costs since only the
25 defective cell has to be replaced and no longer the entire

1 cell stack.

2